

The VDS family of high-speed variable delay lines is available in a dual in-line package for a variety of types in either standard or custom specifications.

**FEATURES**

- High-speed SMD delay lines that have achieved 40 step variability of delay time through a combination of 20 sections of ELMEC's own high-function, high-density delay line elements and high-increment variable structure.
- Suitable for application in a broad range of high-speed logic elements such as the ECL 10KH or 10K series as well as TTL FAST, CMOS FAST and others of similar switching speed.
- They are also suitable for use in a wide range of applications in analog circuits.

**COMMON SPECIFICATIONS**

Inherent Delay:	450ps max. at the minimum point within the variable range
Waveform Distortion:	Overshoot/preshoot under ±20%
Operating Temperature Range:	-10°C to +80°C
Storage Temperature Range:	-40°C to +120°C
Switching Life Expectancy:	Guaranteed within 100 cycles. (One cycle is defined as the movement of the knob from one end to the other.)

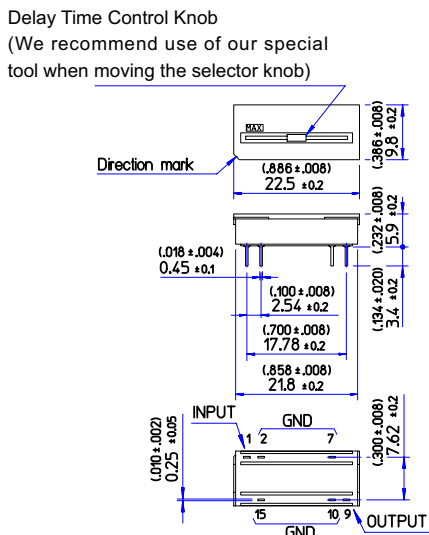


**SPECIFICATIONS**

Part Number	Delay Time Range -0 to +20%	Increment Resolution (40 Steps) * (1)		Rise Time	Input Impedance	Output Impedance	DC Max. Voltage	Preferred Logic Family
		1.75%	3.25%					
VDS5010	0-5ns	88ps	163ps	0.8ns Max. *(2)	50Ω±10%	100Ω±10%	DC 3V Max. Constantly	ECL10KH ECL10K TTL-FAST
VDS1110	0-10ns	175ps	325ps	1.3ns Max. *(2)				
VDS2110	0-20ns	350ps	650ps	2.3ns Max. *(2)				
VDS3110	0-30ns	525ps	975ps	4.0ns Max. *(2)	100Ω±10%	200Ω±10%	DC 4.5V Max. Voltage	CMOS- FACT
VDS5020	0-5ns	88ps	163ps	2.0ns Max. *(3)				
VDS1120	0-10ns	175ps	325ps	2.5ns Max. *(3)				
VDS2120	0-20ns	350ps	650ps	3.5ns Max. *(3)				

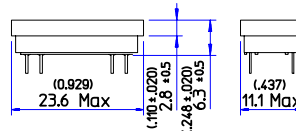
\*(1) Changes at a ratio of 1.75% and 3.25% occur alternately.  
 \*(2) 20%-80%.  
 \*(3) 10%-90%.  
 Delay time temperature coefficient ±100ppm/°C (However, VDS 1110, 2110, 2120, 3110 are -400±200ppm/°C).

**PACKAGE DIMENSIONS & PIN CONFIGURATION**



Unit:mm (inch)

In board design, please note the changes in the dimensions of the VDK Type indicated below when the dust cover cap is attached.



**Application Notes:**

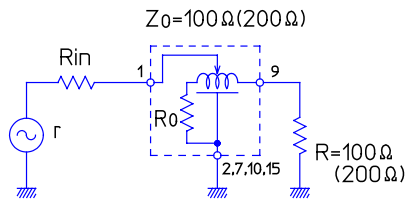
Care is to be exercised in aqueous cleaning since the VDK Type is not hermetically sealed. We recommend hand soldering this part. A dust cover cap is provided on the top of each part.



Note: Published specifications are subject to change without prior notice.

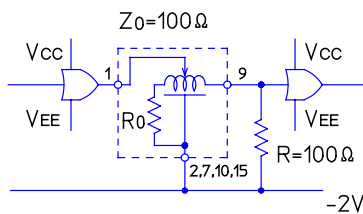
TYPICAL APPLICATIONS AND TERMINATION METHODS

(1) Analog circuit

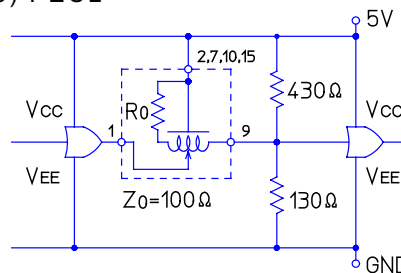


$r$  : Impedance of signal source  
 $R_{in}$ : Input adjustment resistance  
 $Z_0$  : Characteristics impedance of internal Elements (=Output impedance)  
 $R_o$  : Internal adjustment resistance (=Z<sub>0</sub>)  
 $2(r+R_{in})=Z_0=R$

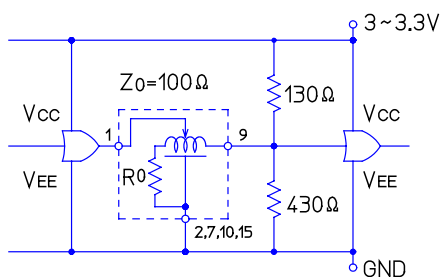
(2) ECL (-2V termination line used)



(3) PECL

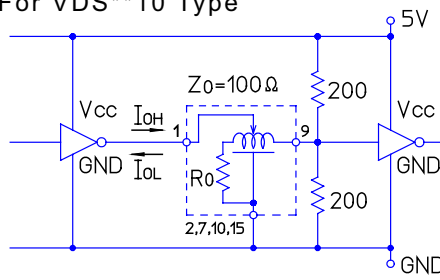


(4) LVPECL



(5) TTL(FAST)

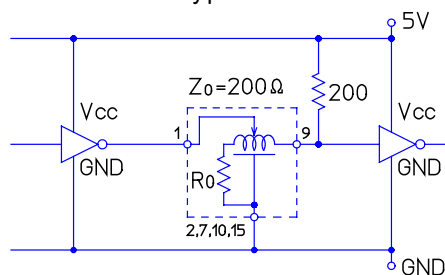
For VDS\*\*10 Type



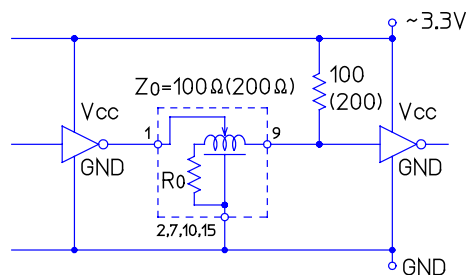
$I_{OH}$  is approx. 45mA,  $I_{OL}$  is approx. 15mA

(6) TTL(FAST)

For VDS\*\*20 Type



(7) CMOS,LVCMOS



RoHS Compliance Status

Compliance Status

RoHS-compliant components are available.