Differential Signal Balancer/Common-mode Noise Absorber CDLD-Type R-Suffix

Multipath Reflection Remover CDLD-Type E-Suffix

1. Features

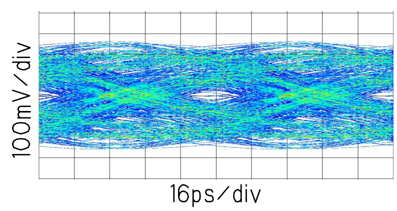
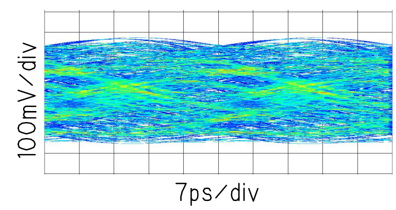
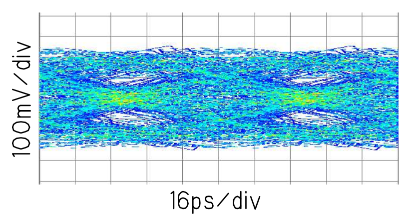
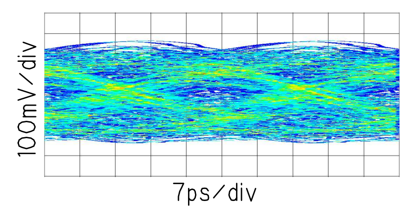
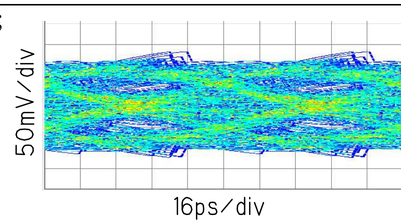
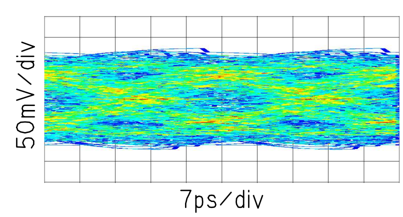
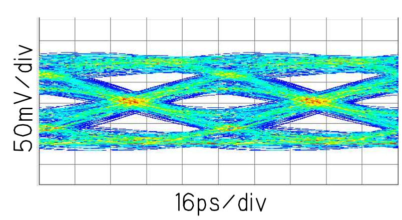
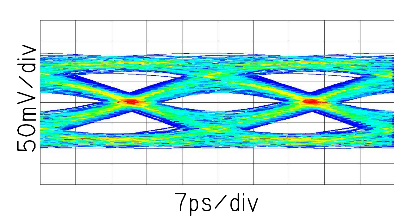
- New, Non-magnetic Common-Mode filter utilizing delay line operating at 4G～28Gbps.
- Restoring Eye Patterns closed due to multipath reflection using the Passive internal CTLE (Continuous Time Linear Equalizer) version. (Please See Technical Note 1)
- Prior Removal and elimination of common-mode noise prevents noise transmission. (Please See Technical Note 2)
- Differential signal inter-phase skew and uneven Rise/Fall are automatically adjusted, correcting balance. (Please See Technical Note 3)

[Application Examples]

- Semi-conductor test device (Gbps) with common-mode noise transmission problems. (Please See Technical Note 4)
- Optical transmission system with an electrical/optical conversion board and high-speed networking device for EMI measure, eye pattern improvement.

This product is a 0805 size multi-layered ceramic chip-type LTCC part and is RoHS-compliant. S-parameter files (Touchstone format) and SPICE models can be provided for each component.

2. 10Gbps Multipath Reflection Removal Example（Please See Technical Note 1）

Load Conditions / Component	12.5Gbps Unbalanced Stray LC	28Gbps Unbalanced Stray LC
Thru		
Thru with Decision Feedback Equalizer (DFE)		
6dB Attenuator with DFE	; 	
CDLD06E (Left) CDLD03E (Right)		

3. Common Specifications

Input/Output Impedance :Differential 100Ω±10% *
Interval Skew Auto-Adjust Time :1/4Pw (Pw Spec: 1Unit Interval pulse width <200ps)
Waveform Distortion :Overshoot/Preshoot under ±20%
Insulation Resistance :DC50V, over 100MΩ
Durable Voltage :DC50V, 1 minute
Rated Current :100mA
Rated Voltage :5V
Operating Temperature Range :−40℃ to +85℃
Storage Temperature Range :−40℃ to +120℃

* Single-ended operation will not produce usable waveforms.

■Multipath Reflection Remover

Part Number	Transmission Speed (1)*	Insertion Loss (2)*	DC Insertion Loss (2)*	Output Rise Time (20%-80%)	Delay Time
CDLD03E (3)*	25G～28Gbps	2dB Typ.(at 13GHz)	5.5dB Typ.	25ps Typ.	30ps Typ.
CDLD04E (4)*	16Gbps	2.5dB Typ.(at 8GHz)	6dB Typ.	30ps Typ.	40ps Typ.
CDLD06E (3)*	10G～12.5Gbps	3dB Typ.(at 6GHz)	6dB Typ.	35ps Typ.	60ps Typ.

■Differential Signal Balancer/Common-mode Noise Absorber

Part Number	Transmission Speed (1)*	-3dB Passband (2)*	Output Rise Time (20%-80%)	Delay Time	DC Resistance
CDLD07R (3)*	16G～28Gbps	DC～20GHz Typ.	25ps Typ.	70ps Typ.	1.0ΩMax.
CDLD10R	8G～16Gbps	DC～15GHz Typ.	30ps Typ.	100ps Typ.	1.5ΩMax.
CDLD15R	5G～12.5Gbps	DC～12GHz Typ.	35ps Typ.	150ps Typ.	1.5ΩMax.
CDLD30R	4G～8Gbps	DC～7.5GHz Typ.	45ps Typ.	300ps Typ.	2.5ΩMax.

(1)* When using the recommended Land Pattern. The case where the passing waveform of 1 unit interval becomes sine wave-like is included. (Please See Technical Note 7)
(2)* When using the recommended Land Pattern.
(3)* Samples available.
(4)* Under development.

[Jumper Features]

After attaching the pads to the printed circuit board, assuming the possibility that this component might not load properly, we have prepared the CDLD00R jumper between the pads.

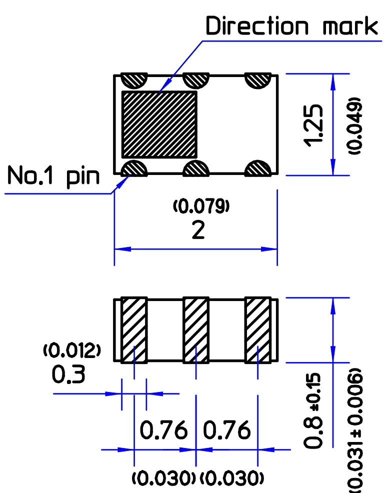
The CDLD00R is utilized for a minimal time between the input and output terminals and has no effect on the reduction of common-mode noise or differential signal balance.

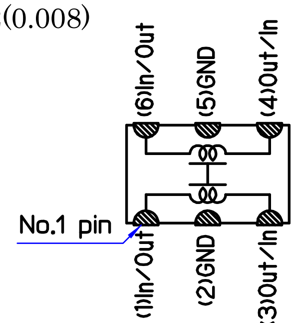
Part Number	-3dB Passband (5)*	Output Rise Time(20%-80%)	Delay Time	DC Resistance
CDLD00R	DC～20GHz Min.	25ps Typ.	10ps Typ.	1.0ΩMax.

(5)* When using the recommended Land Pattern.

4. Package Dimensions and Pin Configuration（provisional）

Unit: mm (inch), Tolerance: ±0.2(0.008)



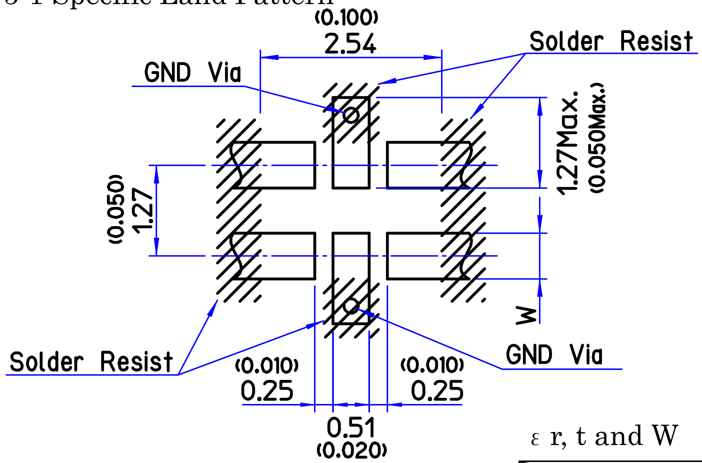


CDLD00R
・No Direction mark
・No connection between 2pin and 5pin

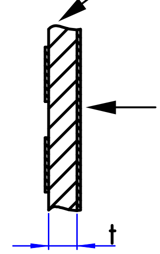
5. Suggested Land Pattern

Unit: mm (inch), Tolerance: ±0.1(0.004)

5-1 Specific Land Pattern



Example for Dielectric Layer

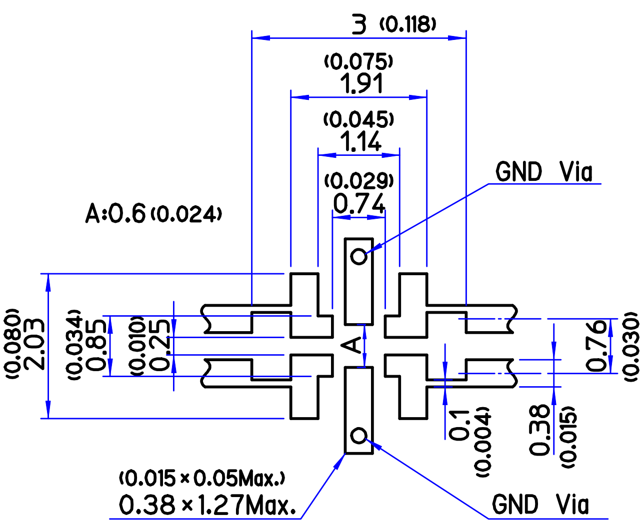


εr, t and W

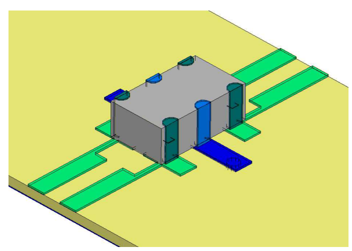
εr \ t	0.3(0.012)	0.4(0.016)	0.5(0.020)
3.5	W=0.56(0.022)	W=0.70(0.028)	W=0.78(0.031)
4.1	W=0.50(0.020)	W=0.64(0.025)	W=0.70(0.028)

5-2 Available Common-mode Choke Coil (0504 size) with shareable Land Pattern

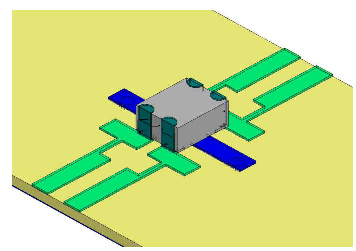
For differential balance improvement and common-mode noise elimination under 10Gbps, an inexpensive common-mode choke coil can even be used. However, considering unanticipated multipath reflection which could occur after production of the board, we recommend insertion of a land pattern which can also be used to mount this product. Below is an example of a land pattern which can also be used with an available 0504 size common-mode choke coil.



w/ this product



w/ 0504 size component



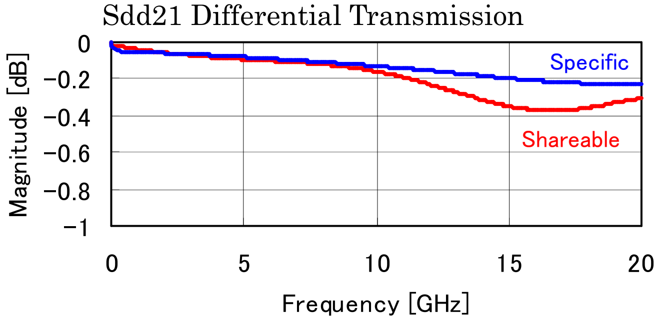
Board measurements
- Thickness : 0.2mm
- εr : 3.1

Please inquire about other board requirements.
0302 size change board is planned.

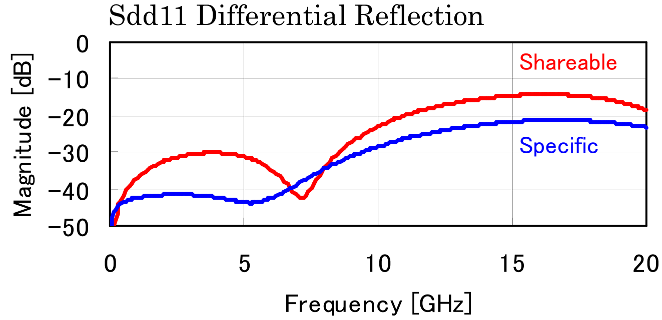
5-3 Quality comparison of Specific Land Pattern and Shareable Land Pattern

(Electromagnetic analysis with loaded CDLD00R.)

Sdd21 Differential Transmission



Sdd11 Differential Reflection

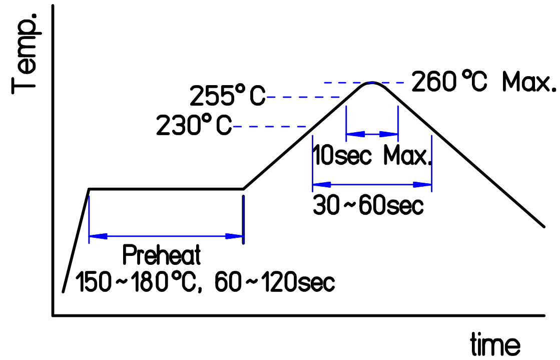


6. Suggested Reflow Soldering Conditions

J-STD-020C Pb-Free Standard

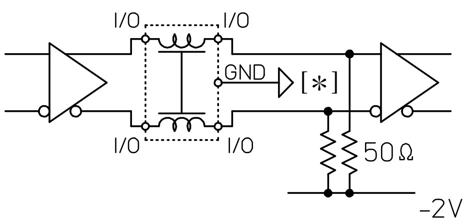
Storage conditions are as per MSL1. These component families are not moisture-sensitive. Baking prior to reflow is not required.

Maximum Cycles: 2x

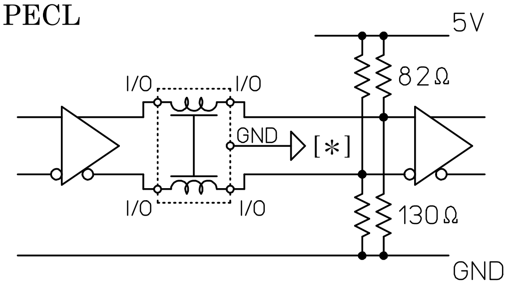


7. Typical Applications

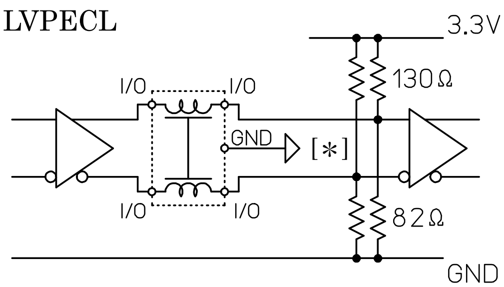
ECL (-2V termination line used)



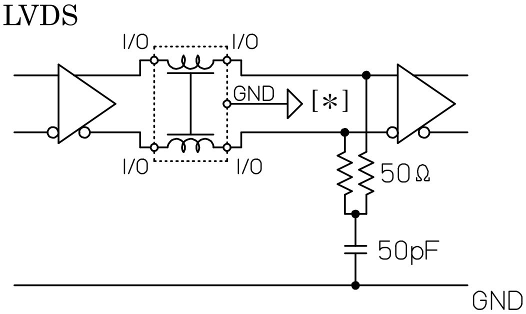
PECL



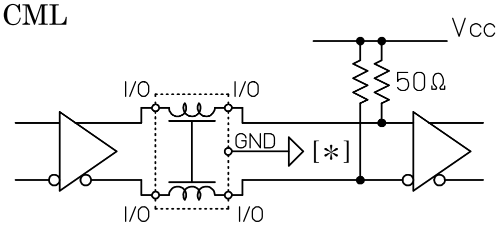
LVPECL



LVDS



CML



[∗] Signal GND potential, such as a power supply GND or a Vcc line.

Please be sure to connect the GND Termination. (Please See Notes)

8. RoHS Compliance Status

RoHS-compliant

9. Notes

Always connect the GND terminals. Using this product without connecting the GND could cause common-mode noise rejection and delay line functions to deteriorate.

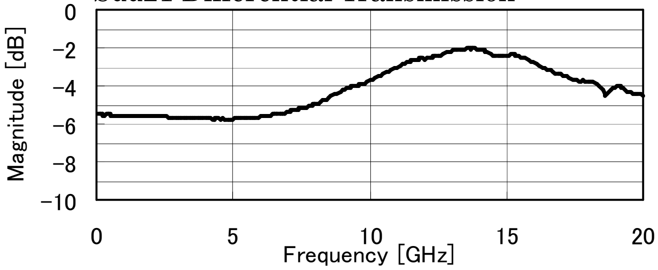
Use of only one line will not yield a normal waveform and cannot be used.

10. Characteristics Examples

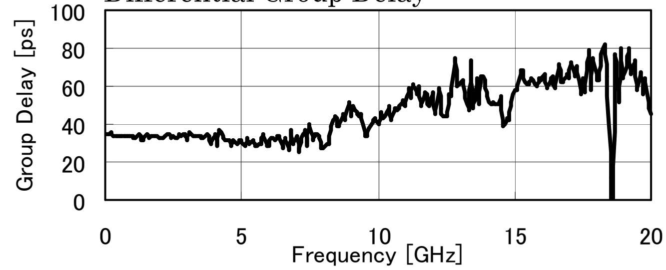
Frequency Characteristics

CDLD03E (Actual Measurement)

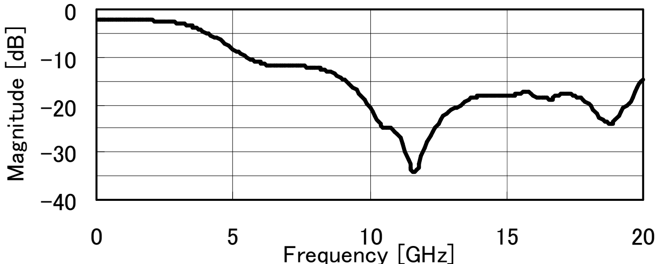
Sdd21 Differential Transmission



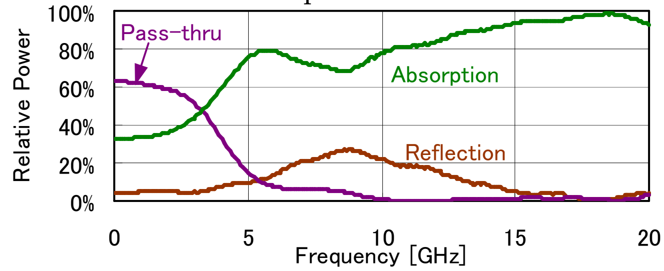
Differential Group Delay



Scc21 Common-mode Transmission

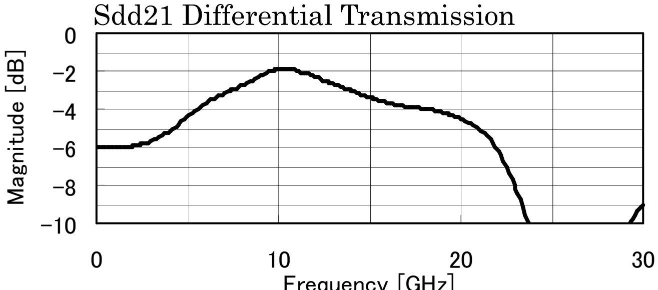


Common-mode power ratio

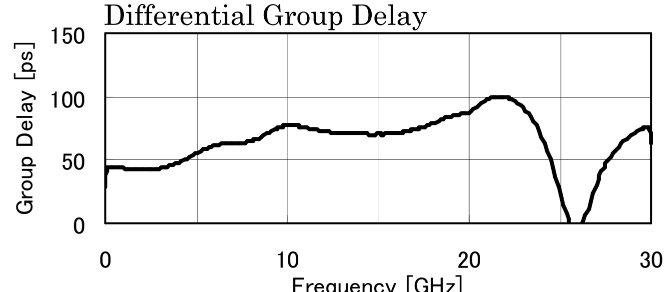


CDLD04E (Electromagnetic Field Analysis)

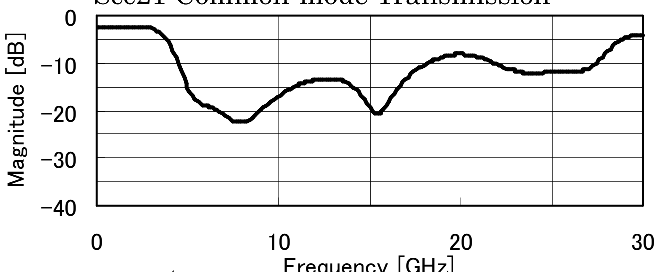
Sdd21 Differential Transmission



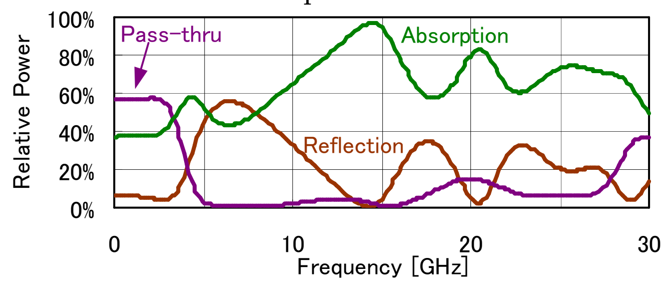
Differential Group Delay



Scc21 Common-mode Transmission

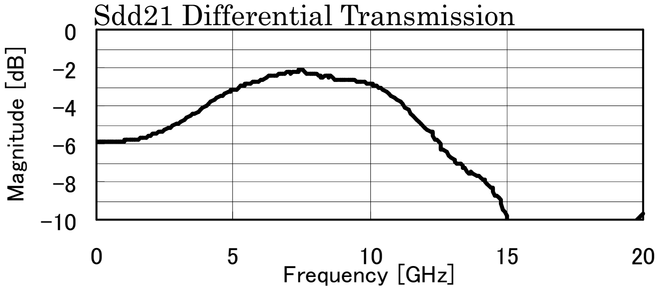


Common-mode power ratio

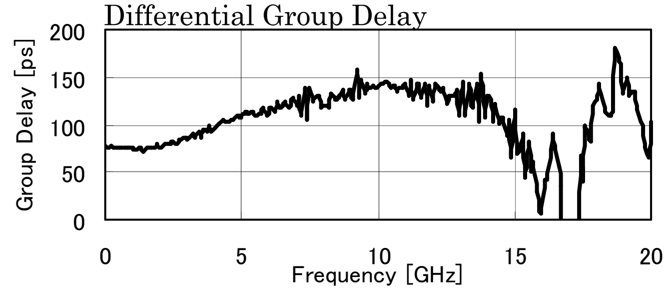


CDLD06E (Actual Measurement)

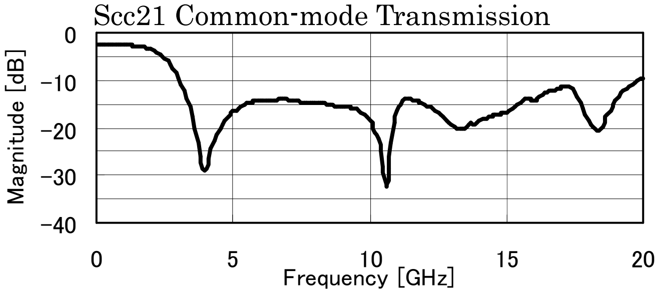
Sdd21 Differential Transmission



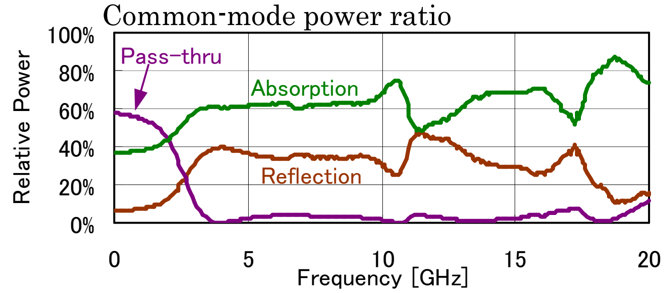
Differential Group Delay



Scc21 Common-mode Transmission

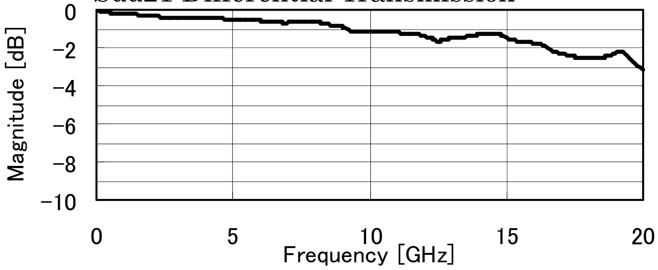


Common-mode power ratio

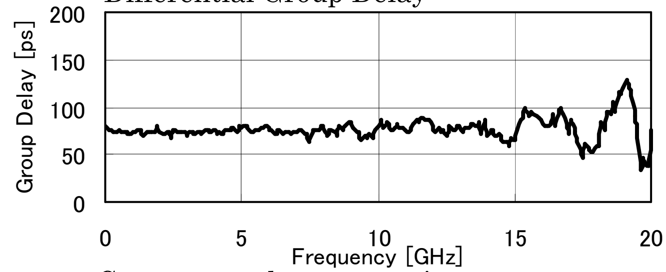


CDLD07R (Actual Measurement)

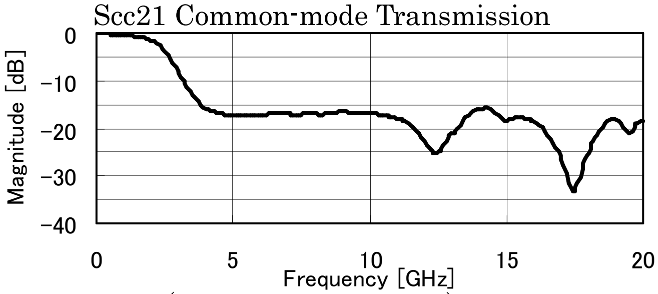
Sdd21 Differential Transmission



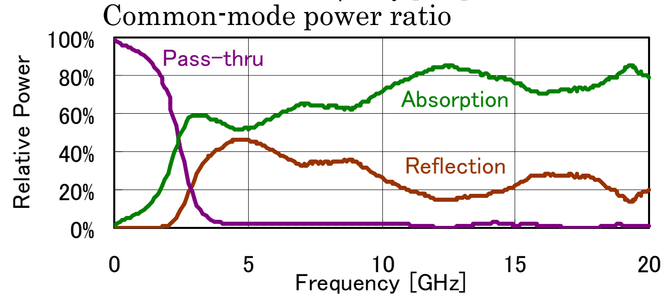
Differential Group Delay



Scc21 Common-mode Transmission

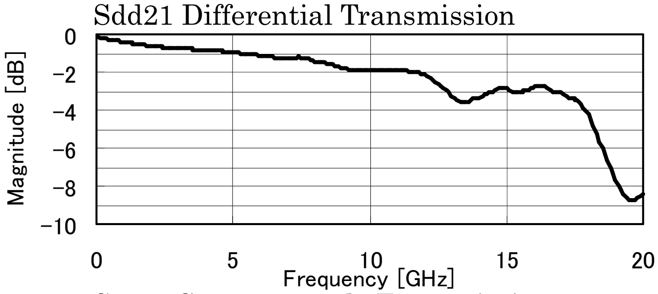


Common-mode power ratio

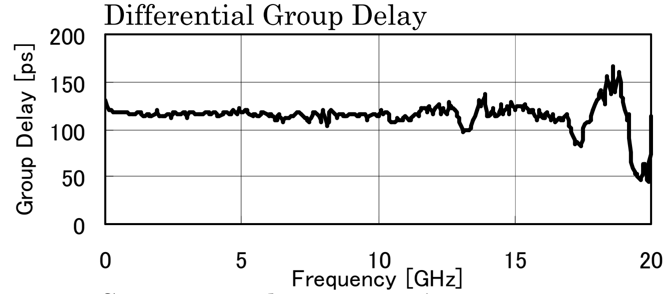


CDLD10R (Actual Measurement)

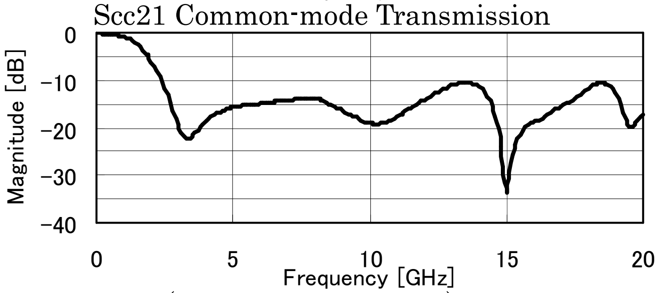
Sdd21 Differential Transmission



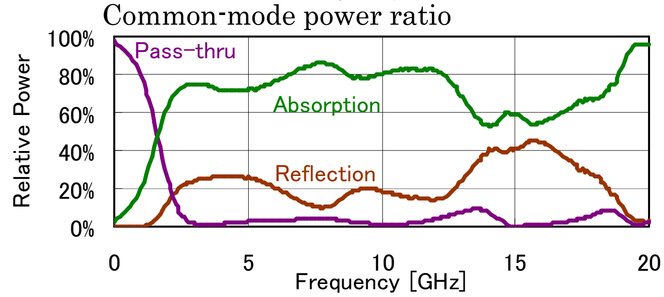
Differential Group Delay



Scc21 Common-mode Transmission

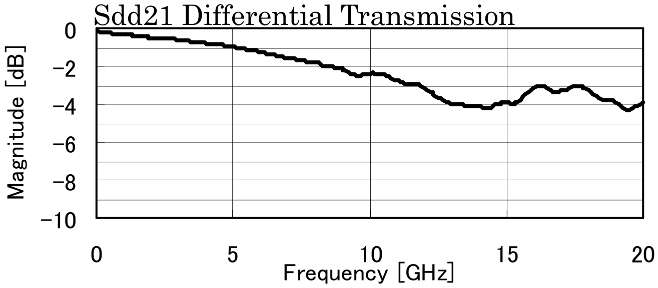


Common-mode power ratio

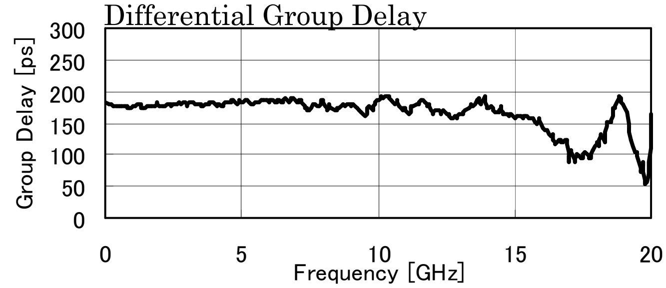


CDLD15R (Actual Measurement)

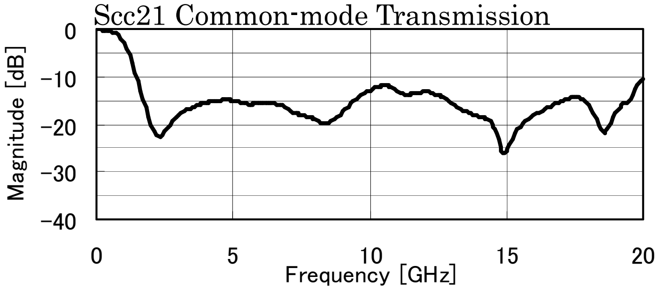
Sdd21 Differential Transmission



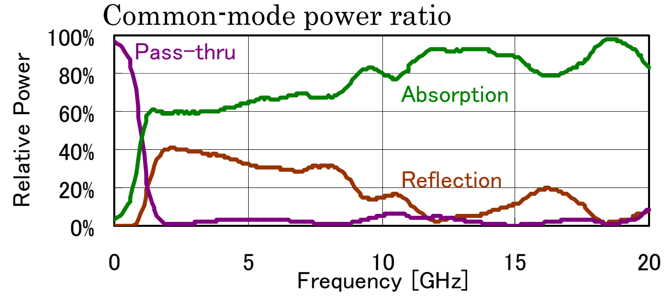
Differential Group Delay



Scc21 Common-mode Transmission

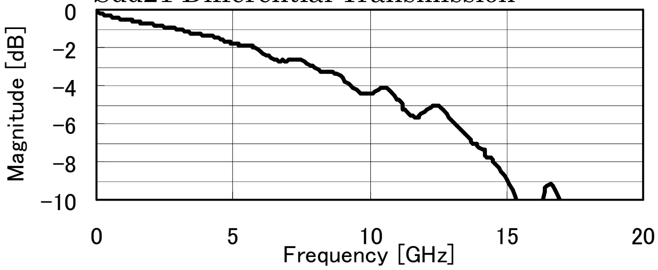


Common-mode power ratio

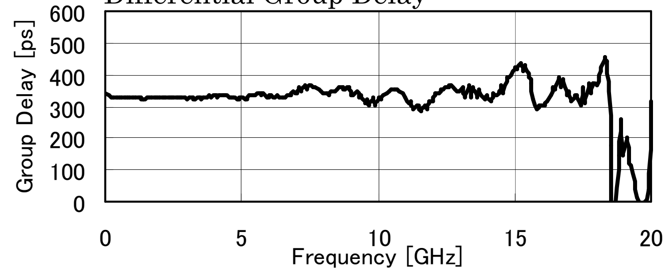


CDLD30R (Actual Measurement)

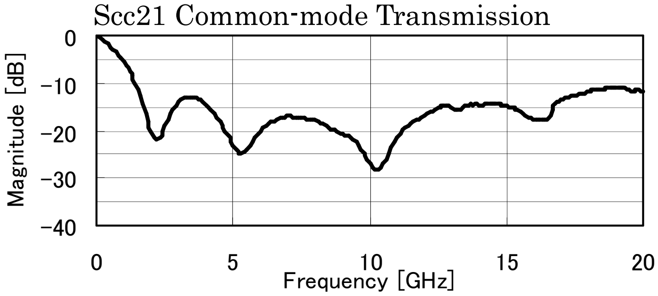
Sdd21 Differential Transmission



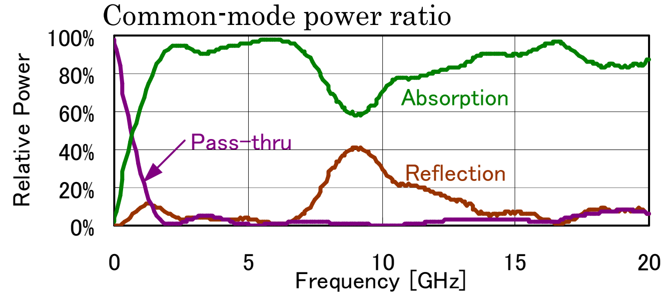
Differential Group Delay



Scc21 Common-mode Transmission



Common-mode power ratio



Pulse response waveform

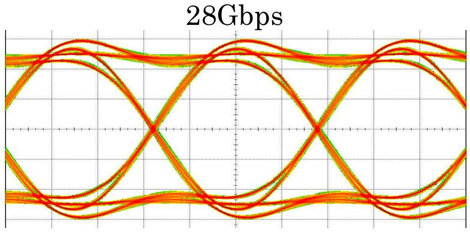
Transient analysis based on actual S-parameter measurements

(Actual data only extends to 20GHz. Due to lack of band-width, S-parameter was used for the electromagnetic field analysis at 28Gbps and 16Gbps.)

Skew of Input Pseudo-Random Bit Sequence: 0ps

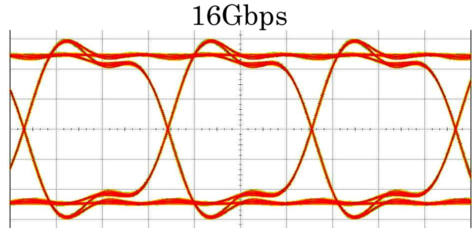
CDLD07R

28Gbps



X-axis: 10ps/div
Y-axis: 200mV/div

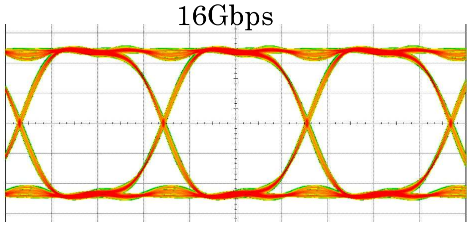
16Gbps



X-axis: 20ps/div
Y-axis: 200mV/div

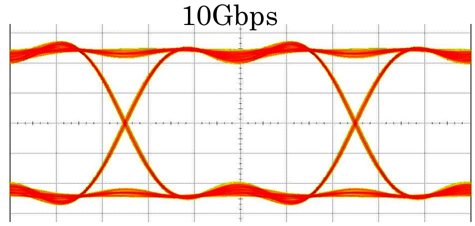
CDLD10R

16Gbps



X-axis: 20ps/div
Y-axis: 200mV/div

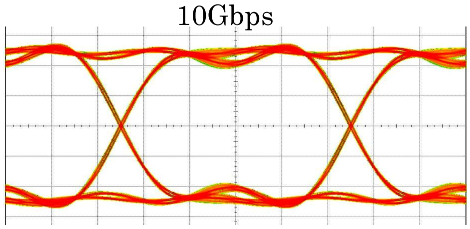
10Gbps



X-axis: 20ps/div
Y-axis: 200mV/div

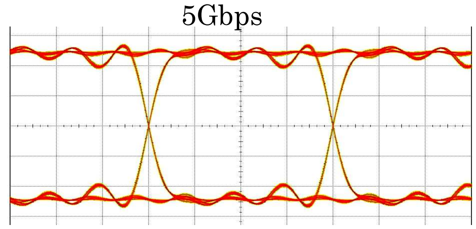
CDLD15R

10Gbps



X-axis: 20ps/div
Y-axis: 200mV/div

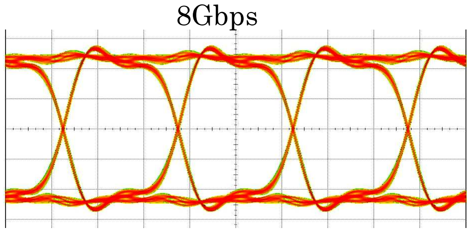
5Gbps



X-axis: 50ps/div
Y-axis: 200mV/div

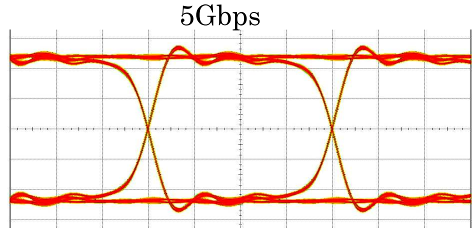
CDLD30R

8Gbps



X-axis: 50ps/div
Y-axis: 200mV/div

5Gbps

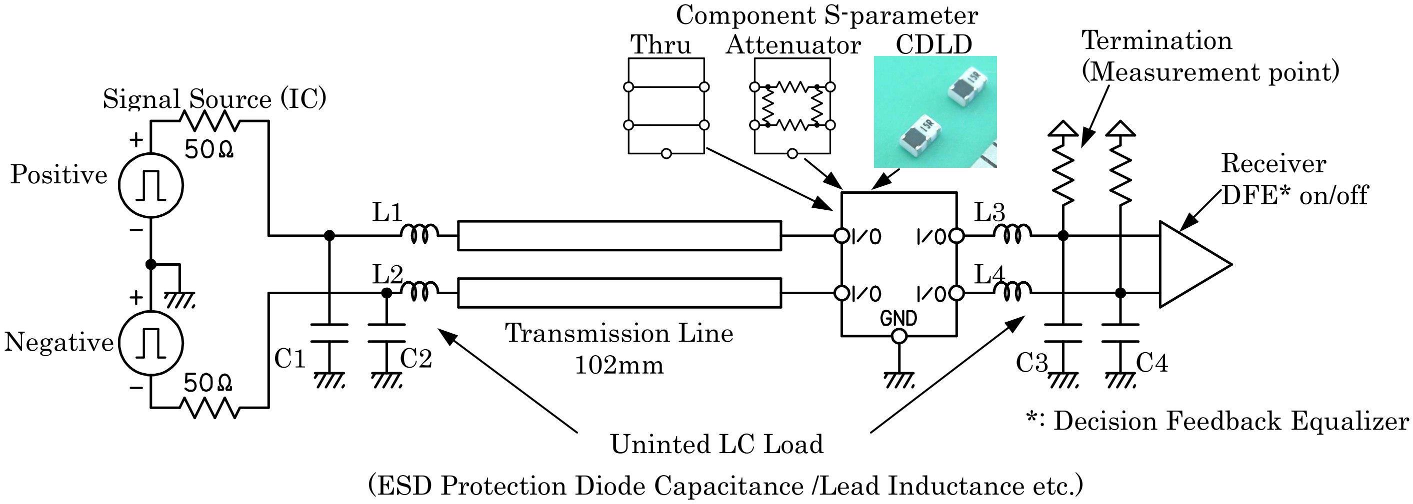


X-axis: 50ps/div
Y-axis: 200mV/div

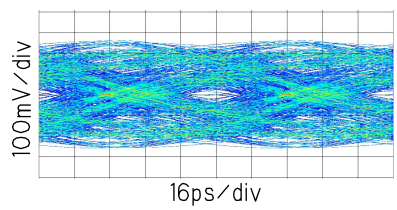
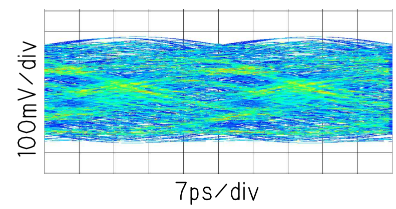
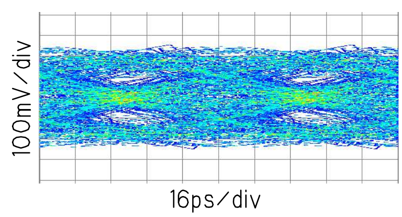
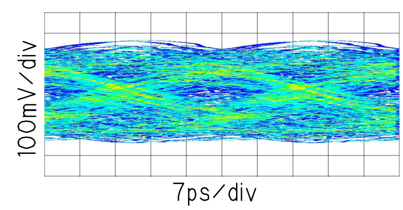
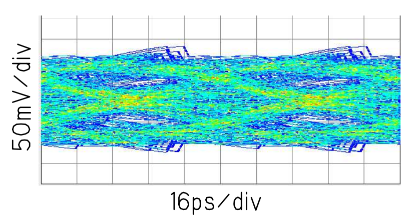
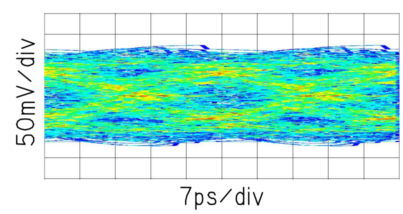
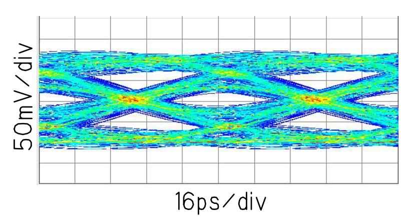
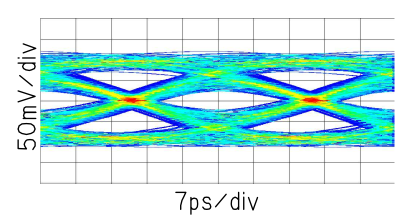
Technical Note 1: Example of Eye-Pattern Improvement/Multipath Reflection Removal

For transmission rates over 10Gbps, multipath reflection is generated from the capacitive load of IC's ESD protection diode and pad which can cause deterioration of the eye pattern. Also, unintended unbalanced capacitive/inductive load should also be considered. Differential eye patterns connected with various capacitive/inductive loads are shown form a circuit simulation using the circuit shown below.

In spite of the capacitive/inductive load, it is possible to remove multipath reflection and improve a stable eye pattern with the CDLD type.



12.5Gbps/28Gbps Pseudo-Random Bit Sequence (PRBS)

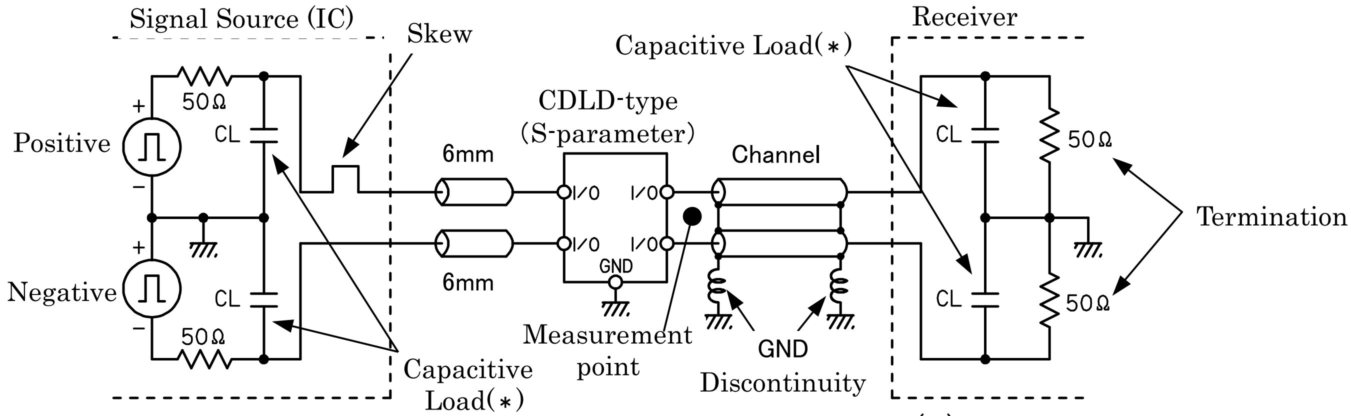
Load Conditions / Component	12.5Gbps Unbalanced Stray LC L1/C1 & L4/C4 : 2nH/2pF L2/C2 & L3/C3 : 1nH/1pF	28Gbps Unbalanced Stray LC L1/C1 & L4/C4 : 0.75nH/0.75pF L2/C2 & L3/C3 : 0.25nH/0.25pF
Thru (2) (without DFE)		
Thru (2) with DFE		
6dB Attenuator (2) with DFE	; 	
CDLD06E (Left) (1) CDLD03E (Right)(1) (without DFE)		

(1)* S-parameter from Actual Measurement
(2)* S-parameter from Circuit Simulator

<u>Technical Note 2: Example of Common-Mode Noise Elimination</u>

For transmission speeds in excess of 10Gbps, even a minor skew will cause common-mode noise. Below is the circuit used to produce the common-mode noise wave form.

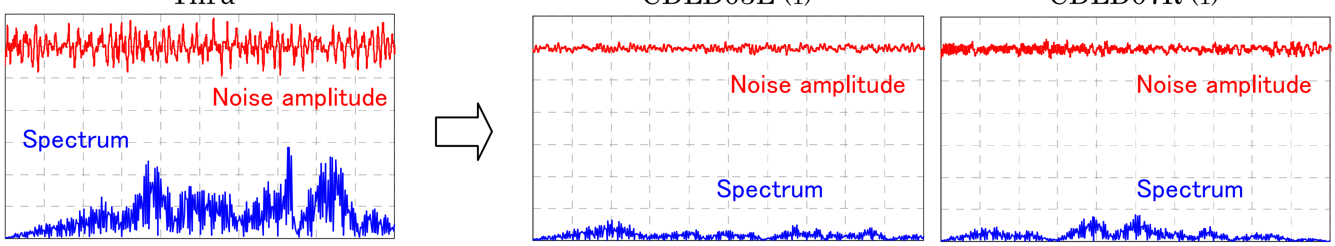
A CDLD-type is inserted directly after the IC, the GHz band common-mode noise is eliminated and transmission noise is prevented from returning to the original level.



(∗) ESD Protection Diode etc.

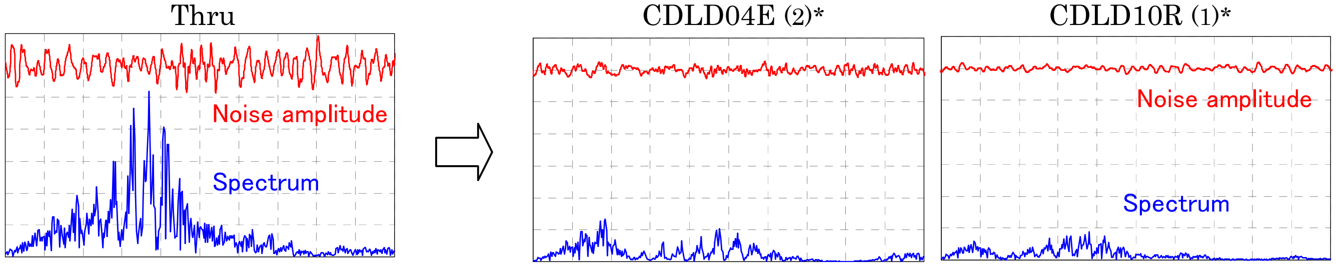
(A) 28Gbps Pseudo-Random Bit Sequence, Skew:10ps, CL:0.5pF, Channel Length:30mm

Thru / CDLD03E (1)* / CDLD07R (1)*



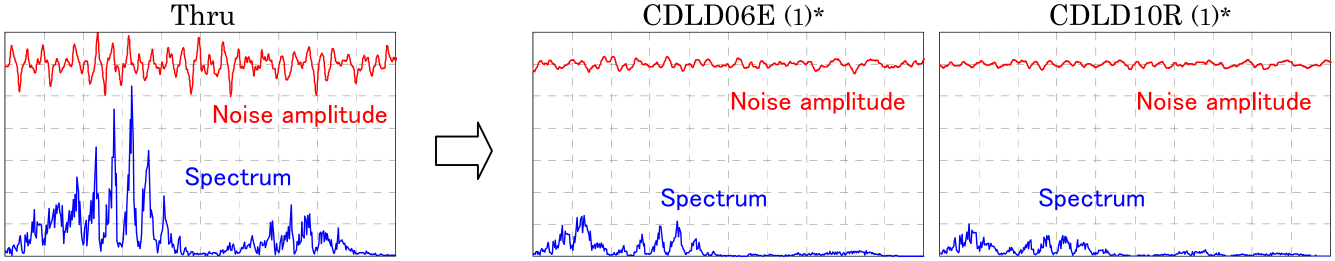
(B) 16Gbps Pseudo-Random Bit Sequence, Skew:20ps, CL:1.0pF, Channel Length:100mm

Thru / CDLD04E (2)* / CDLD10R (1)*



(C) 10Gbps Pseudo-Random Bit Sequence, Skew:25ps, CL:1.5pF, Channel Length:100mm

Thru / CDLD06E (1)* / CDLD10R (1)*



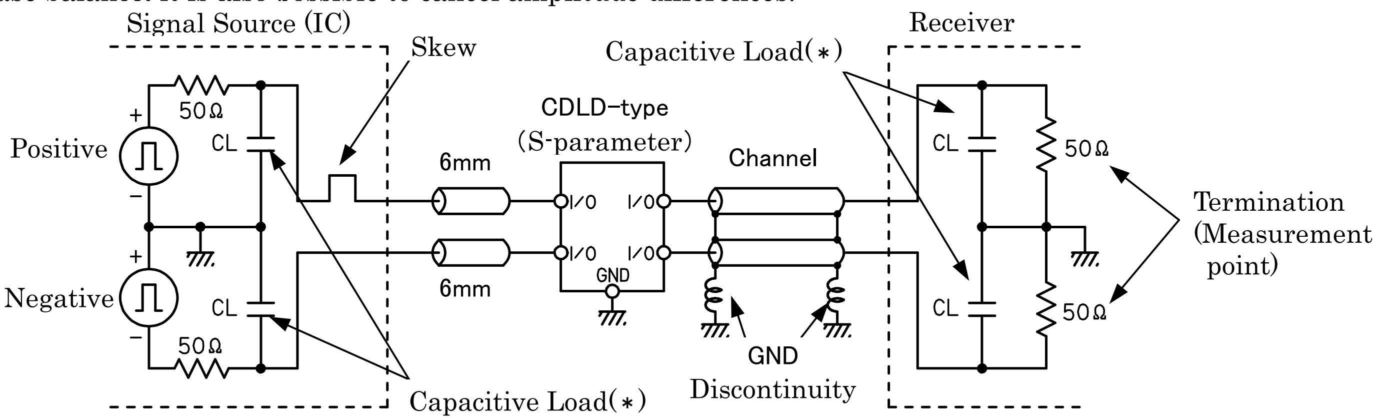
ALL Graph Noise amplitude[X-axis:500ps/div,Y-axis:500mV/div], Spectrum[X-axis:2GHz/div,Y-axis:10mV/div]

(1)* S-parameter Actual Measurement
(2)* S-parameter Electromagnetic Field Analysis

Technical Note 3: Example of Differential Signal Balance Improvement

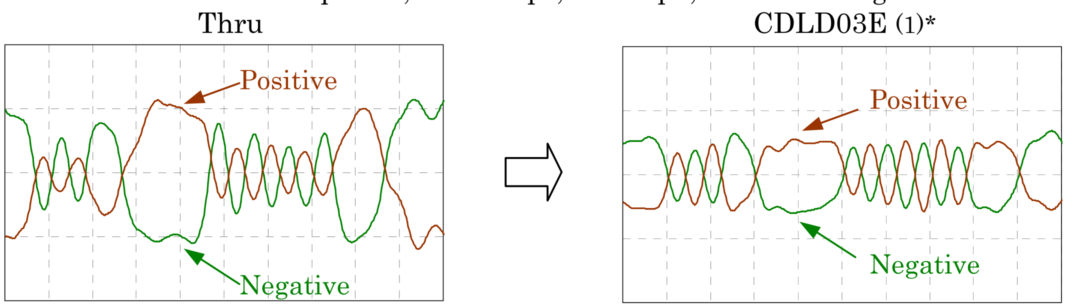
The wave form at the receiver will degrade due to skew or a connector GND discontinuity. The positive/negative differential signal wave forms of such a case are shown using the circuit below.

By using the CDLD with a passive internal CTLE, in addition to skew cancelation and improvement of the phase balance, it is also possible to cancel amplitude differences.



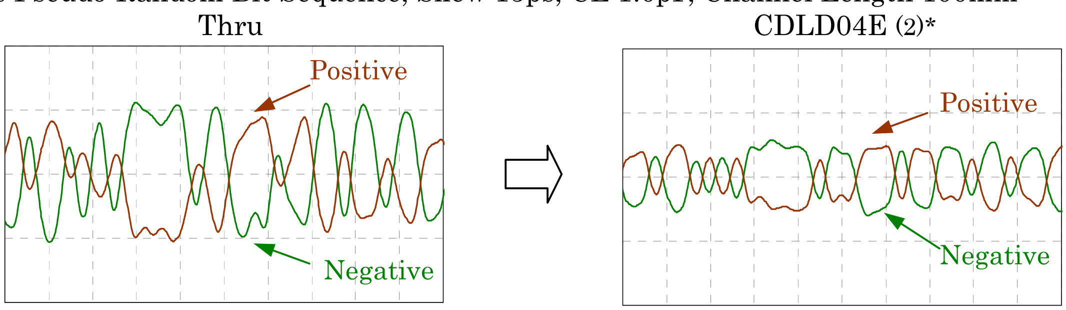
(∗) ESD Protection Diode etc.

(A) 25Gbps Pseudo-Random Bit Sequence, Skew:10ps, CL:0.5pF, Channel Length:30mm



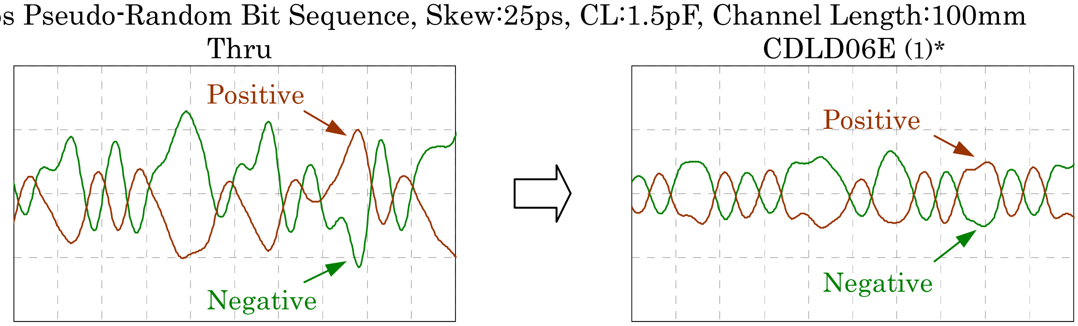
[X-axis:100ps/div, Y-axis:500mV/div]

(B) 16Gbps Pseudo-Random Bit Sequence, Skew:15ps, CL:1.0pF, Channel Length:100mm



[X-axis:200ps/div, Y-axis:500mV/div]

(C) 10Gbps Pseudo-Random Bit Sequence, Skew:25ps, CL:1.5pF, Channel Length:100mm



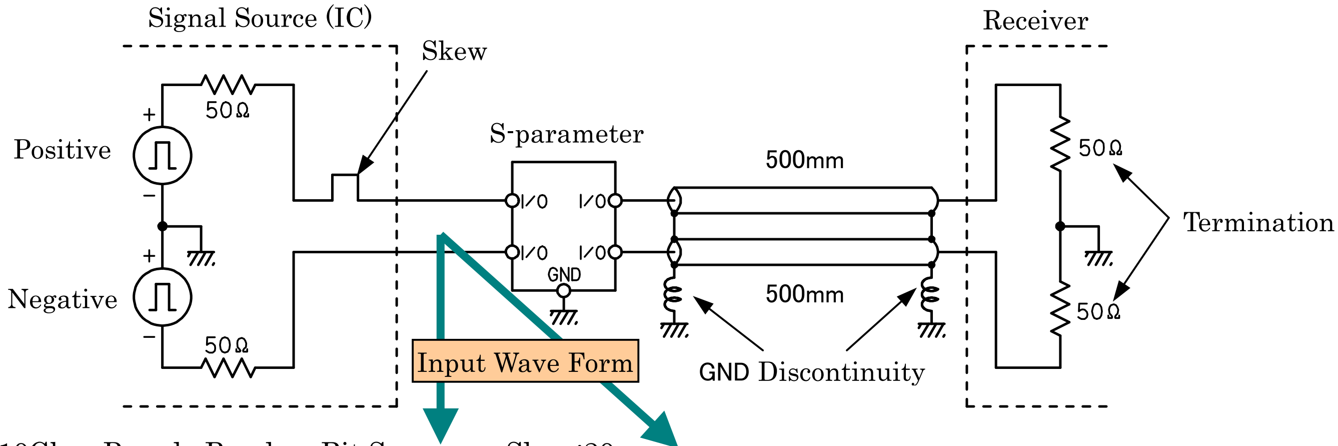
[X-axis:200ps/div, Y-axis:500mV/div]

(1)* S-parameter Actual Measurement
(2)* S-parameter Electromagnetic Field Analysis

Technical Note 4: Comparison of Common-mode Noise Input Reflection

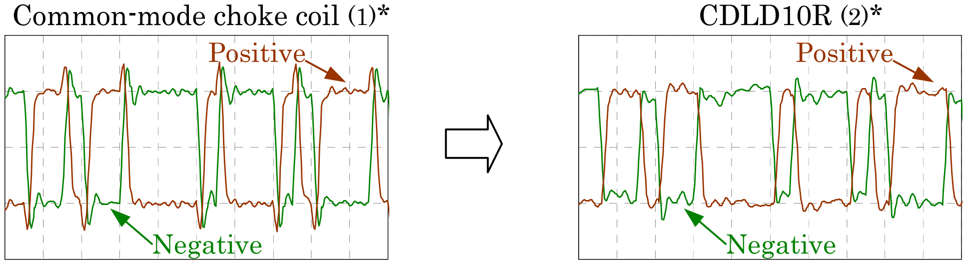
For transmission speeds under 10Gbps, Common-mode Choke Coils are available; however, the reflection from the Common-mode Noise which is blocked by the Common-mode Choke Coil is quite large, the spike on the input wave form from the reflected Common-mode Noise will be superimposed. Using a comparator to compare the input and output wave forms, this superimposed noise can be quite detrimental. The positive/negative input wave forms of such a case are shown using the circuit below.

The CDLD-type's ability to absorb the Common-mode Noise in the GHz band is quite high which prevents the superimposition of Common-mode Noise reflections on the input wave form.



(A) 10Gbps Pseudo-Random Bit Sequence, Skew:20ps

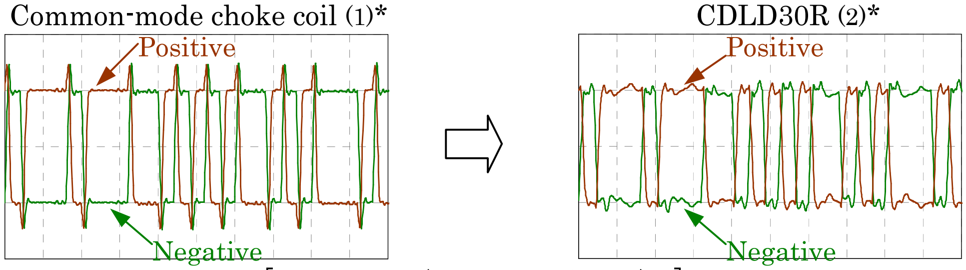
Common-mode choke coil (1)* CDLD10R (2)*



[X−axis:200ps/div, Y−axis:500mV/div]

(B) 5Gbps Pseudo-Random Bit Sequence, Skew:30ps

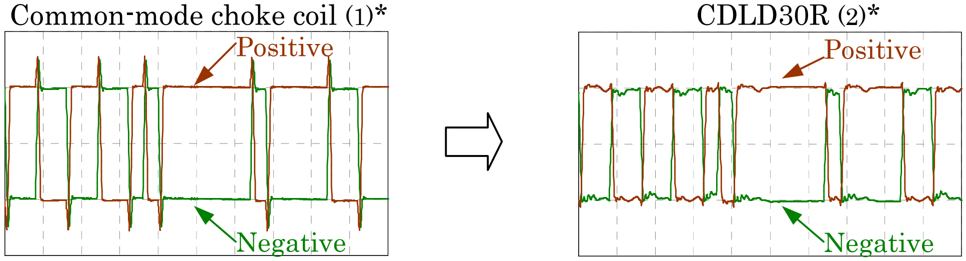
Common-mode choke coil (1)* CDLD30R (2)*



[X−axis:500ps/div, Y−axis:500mV/div]

(C) 2.5Gbps Pseudo-Random Bit Sequence (3)*, Skew:50ps

Common-mode choke coil (1)* CDLD30R (2)*



[X−axis:1ns/div, Y−axis:500mV/div]

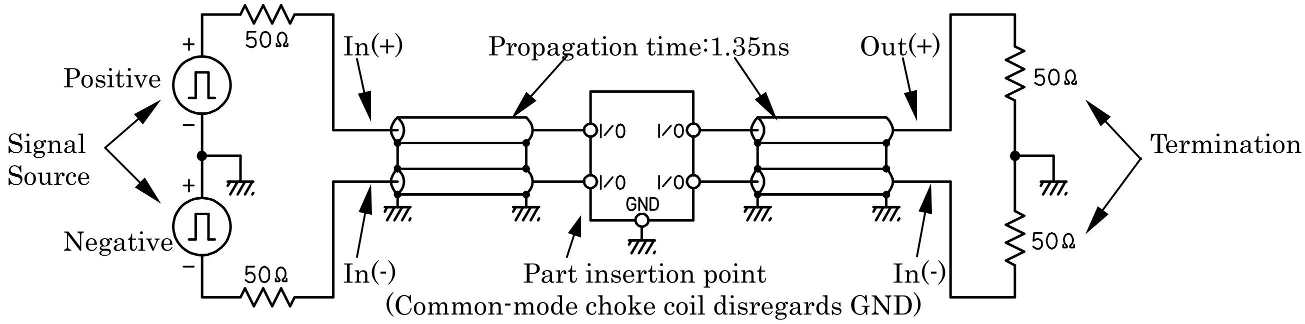
(1)* Equivalent circuit created by a circuit simulator.

(2)* S-parameter Actual Measurement.

(3)* CDLD30R corresponding transmission speed is 4G～8Gbps; however, when used to prevent Common-mode Noise reflection, depending on the frequency of the noise, effectiveness at lower transmission speeds is also shown.

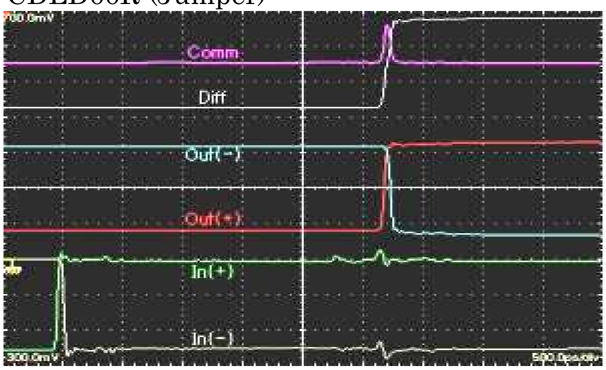
Technical Note 5: Step Response Skew Improvement Example

Using a TDR Sampling Oscilloscope, we constructed and measured the test circuits shown below, positive/Negative (In(+)/In(-)/Out(+)/Out(-)), output common-mode noise (Comm) and the output differential signal (Diff) step response wave forms are shown. The CDLD-type, which contains a delay mechanism, delays the noise from the output waveform and avoids affecting the rise/fall edge.



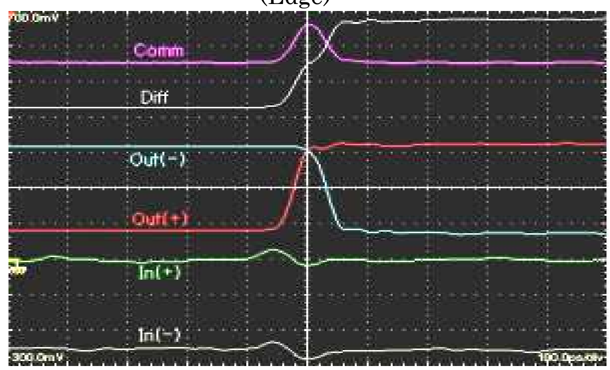
Skew of signal source: 60ps

(A) CDLD00R (Jumper)



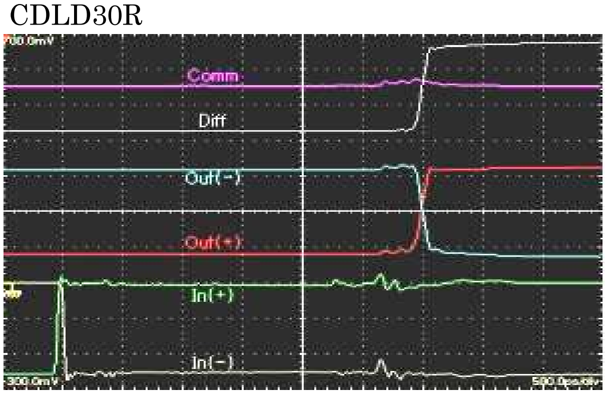
[X-axis:500ps/Div]

(Edge)



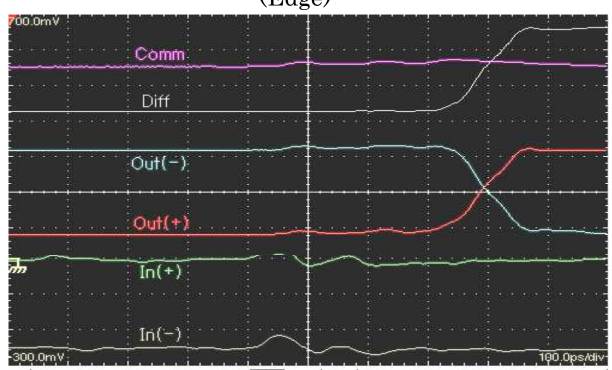
[X-axis:100ps/Div]

(B) CDLD30R



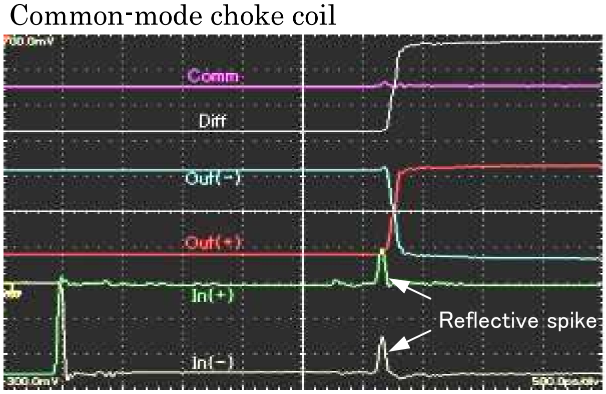
[X-axis:500ps/Div]

(Edge)



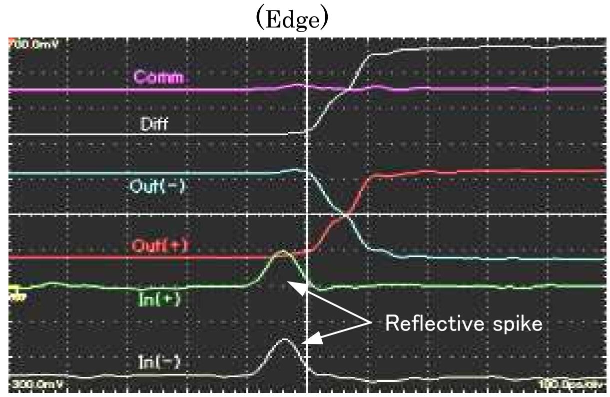
[X-axis:100ps/Div]

(C) Common-mode choke coil



[X-axis:500ps/Div]

(Edge)



[X-axis:100ps/Div]

ALL Graph In/Out/Comm[Y-axis:100mV/Div], Diff[Y-axis:200mV/Div]

Technical Note 6: Frequency Characteristics of Common-Mode Impedance

For the CDLD-type and the ideal common-mode choke coil (hereafter, ideal CMC), the frequency characteristics of common-mode impedance are calculated with a circuit simulator and the difference is verified. The equivalent circuit and the main characteristics of the ideal CMC are shown in Fig. 1. As much as possible, the −3dB passband was made wideband.

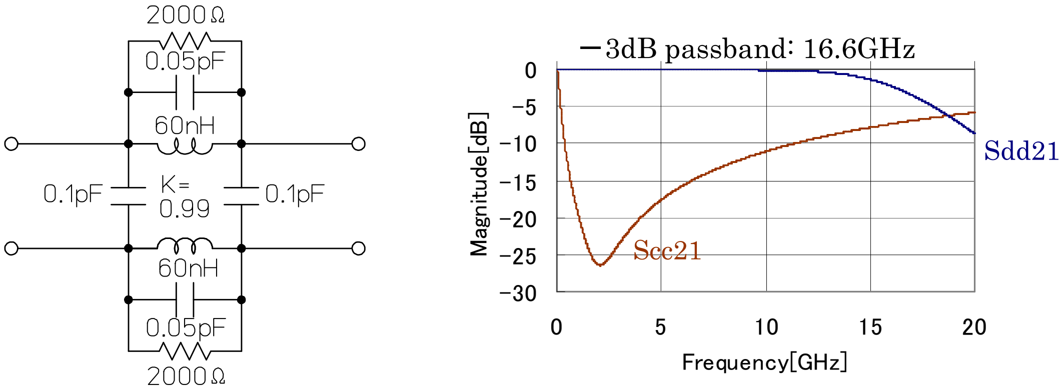


Fig.1 Equivalent circuit and main characteristics of the ideal CMC

The method utilized for calculating common-mode impedance is shown below.

In general, common-mode impedance (Zcom) Fig. 2, is generated by a common-mode choke coil from common-mode noise. That value can be calculated from this circuit. Conversely, because the structure of the CDLD-type absorbs and removes the common-mode noise within the Signal Line-GND circuit, common-mode impedance (Zcom) can be calculated from the circuit arranged and shown in Fig. 3.

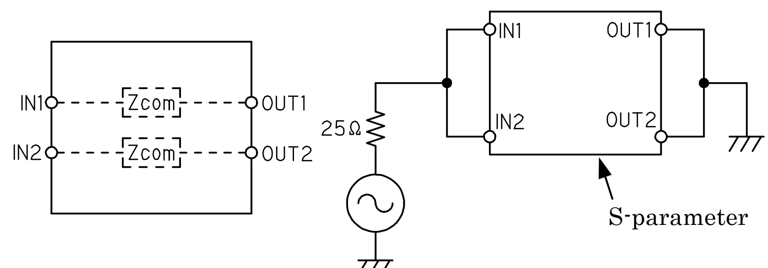


Fig.2 Generation chart and calculation common-mode choke coil Zcom

Fig. 4 shows the frequency characteristics of the ideal CMC and CDLD30R Common-mode impedance from the calculation circuits in Figs. 2 and 3. Here, the ideal CMC uses a circuit simulation S-parameter while the CDLD30R uses an S-parameter measured with a 4-port network analyzer.

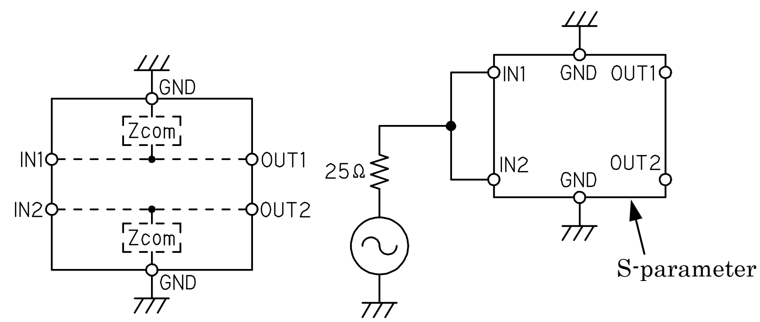


Fig.3 Generation chart and calculation circuit of CDLD type Zcom

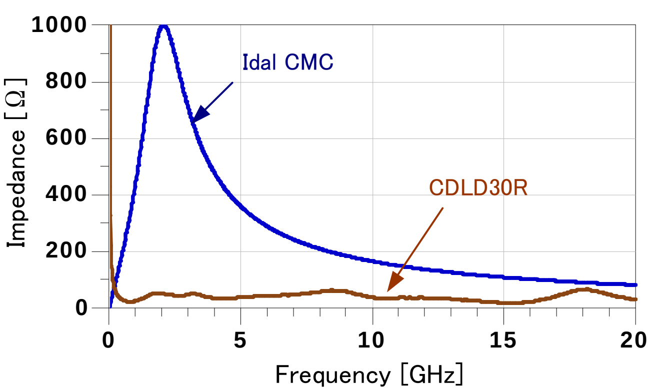


Fig.4 Frequency characteristics of Common-mode impedance

The ideal CMC intercepts the common-mode noise by generating high impedance within the signal line. As shown in Fig. 4, it appears to be effective in the vicinity of 2GHz. However, the inclination of the frequency characteristics is quite steep. Common-mode impedance is reduced as it diverges from 2GHz, and the intercept function decreases.

On the other hand, the CDLD30R is set to the value from the signal-GND circuit corresponding to the common-mode impedance which is constant and small and has a fairly smooth frequency response. There appears to be an advantage to being able to lower the dependency on the frequency and to do a wideband absorptive removal of the common-mode noise.

Technical Note 7: CDLD Transmission Speed

The differential frequency characteristics (Sdd21) of a differential transmission line with a 30ps skew are shown in Fig. 1. In Fig. 1, a differential signal is intercepted to become a complete common-mode signal at 16.7GHz because the 30ps skew makes a 180° phase shift at that frequency. Transmission of the differential signal forms an attenuation pole at 16.7GHz and the －3dB passband becomes DC to 8.3GHz.

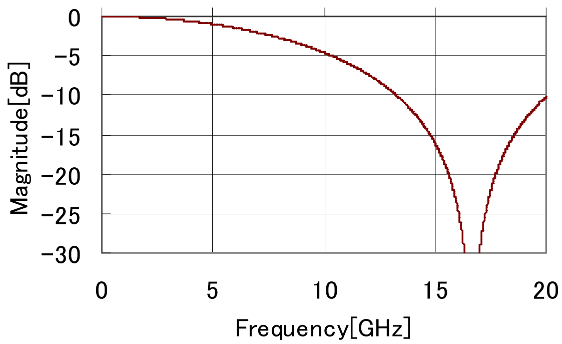


Fig. 1 Differential frequency characteristics (Sdd21) of differential transmission line with 30ps Skew

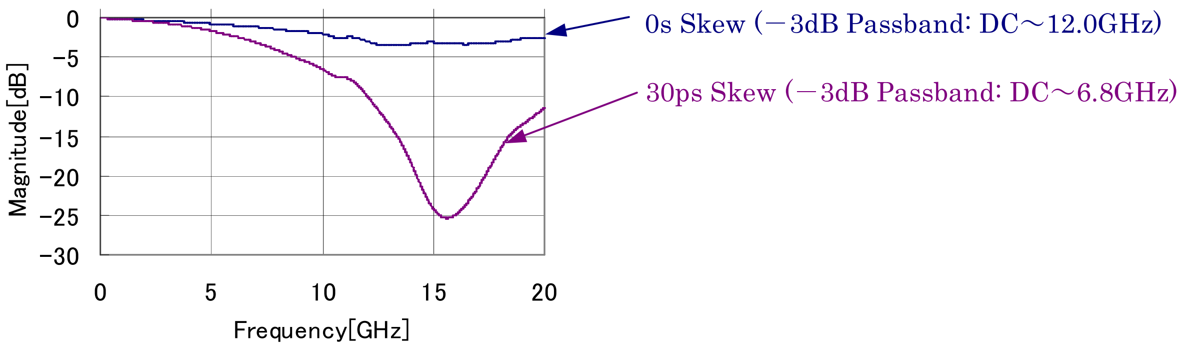


Fig.2 Differential frequency characteristics (Sdd21) with CDLD15R connected in the differential transmission line shown in above.

Next, the CDLD15R frequency characteristics of the differential input signal skew of 0s, 30ps are shown in Fig. 2.

In Fig. 2, compared to the －3dB passband of 0s skew, the －3dB passband of 30ps skew is greatly reduced. However, as clearly indicated in Fig. 1, the cause is not due to the effects of the CDLD15R; rather, it is determined by skew generated by the transmission line. That is, the quality of the differential output waveform probably does not depend on the CDLD －3dB passband. Rather, it depends on the value of the skew when the CDLD is connected for skew cancellation. It can be assumed to become like the sine wave to which the high-order harmonic is missed in 1Unit Interval corrugating according to the transmission speed. Especially at speeds of more than 10Gbps, the trend is more noticeable.

Therefore, the corresponding transmission speed of CDLD is not calculated simply from its －3dB passband, when the skew was generated, the maximum value at the correspondence transmission speed to which output waveform fineness was able to be maintained was examined on the assumption that passing waveform at 1Unit Interval became like the sine wave according to the characteristic of Fig. 1.

As a result, we judged that it was possible to correspond enough up to the transmission speed described in the specifications.

In addition, our CSKF-type not only cancels the skew but also restores the differential transmission signal. If the rough skew is canceled by the CSKF-type and the residual skew is canceled by the CDLD, it is possible to balance the differential signal completely.